DEPARTMENT OF SCIENCE

COURSE OUTLINE – WINTER 2021

CS3290 (A3): COMPUTER ORGANIZATION AND ARCHITECTURE II – 3 (3-0-3)
90 Hours over 15 Weeks

INSTRUCTOR:	Libero Ficocelli	**PHONE:**	780 539-2825
OFFICE:	C424	**E-MAIL:**	LFicocelli@gprc.ab.ca
OFFICE HOURS:	TBA		

WINTER 2021 DELIVERY:
Mixed Delivery – Remote and Onsite. This course is delivered remotely with some face-to-face/onsite components at the GPRC Grande Prairie campus.
For the remote delivery components:

- students must have a computer with a webcam and reliable internet connection. Technological support is available through helpdesk@gprc.ab.ca.
- For the onsite components: students must supply their own mask [and/or face shield] and follow GPRC Campus Access Guidelines and Expectations.

Note: GPRC reserves the right to change the course delivery.

CALENDAR DESCRIPTION:
Digital circuits, combinational systems, memory, register transfer, control logic design, CPU design, and advanced topics on micro-architectures.

PREREQUISITE(S)/COREQUISITE: CS2290 or permission of the instructor

REQUIRED TEXT/RESOURCE MATERIALS:

I will be providing links to several OER textbooks as well as additional resource material

Optional Text :

Logic and Computer Design Fundamentals 5th edition (older editions acceptable)
Morris Mano, Charles Kime, Tom Martin
Pearson Education

DELIVERY MODE(S): In class lecture

COURSE OBJECTIVES:

Students will be introduced to digital computer architecture and its underlying digital logic including topics such as:

- integrated circuits from basic logic gates to more complex chips (registers and ALUs)
- fundamentals of digital logic analysis and design.
- Boolean Algebra and its relation to circuit design and minimization
- combinational (no memory component) and sequential (memory) logic
- single bit memory to more organized memory such as registers.
- data paths, control unit design and generic CPU design.

LEARNING OUTCOMES:

Students will be able to:

- Understand and manipulate Boolean logic
- Design and build combinational circuits to perform a variety of tasks
- Design and build sequential circuits to perform a variety of tasks
- Reduce both sequential and combinational circuits
- Build a simple CPU which will include registers, ALU, data path and all the necessary circuitry required to decode and execute program code presented in a binary format.

TRANSFERABILITY:

Please consult the Alberta Transfer Guide for more information. You may check to ensure the transferability of this course at the Alberta Transfer Guide main page http://www.transferalberta.ca.

** Grade of D or D+ may not be acceptable for transfer to other post-secondary institutions. **Students are cautioned that it is their responsibility to contact the receiving institutions to ensure transferability**

EVALUATIONS:

	Original
Lab/Homework Assignments	30%
Class Quizzes	10%
Midterm	25%
Final Exam	35%

GRADING CRITERIA:

Please note that most universities will not accept your course for transfer credit **IF** your grade is **less than C-**.

Alpha Grade	4-point Equivalent	Percentage Guidelines		Alpha Grade	4-point Equivalent	Percentage Guidelines
A+	4.0	90-100		C+	2.3	67-69
A	4.0	85-89		C	2.0	63-66
A-	3.7	80-84		C-	1.7	60-62
B+	3.3	77-79		D+	1.3	55-59
B	3.0	73-76		D	1.0	50-54
B-	2.7	70-72		F	0.0	00-49

COURSE SCHEDULE/TENTATIVE TIMELINE:

- Boolean Algebra (basic identities, algebraic manipulation)
- Logic gates
- Canonical Forms (minterms, maxterms, SOP, POS)
- Applications of Boolean Algebra
- Karnaugh Maps (2,3,4,5 variable maps, implicants prime/essential, covering set)
- Quine-McCluskey Method
- Decoders/Encoders/Priority Encoders (decoder expansion)
- Multiplexers/Demultiplexer (use of MUX in Boolean Function Implementation)
- Latches/Flip-Flops (S-R, D, J-K, Master-Slave, Edge triggered)
- Sequential Circuits (Characteristic/Excitation Tables, state diagrams, analysis and design)
- Mealy/Moore Machines,
- State Minimization
- Counters (Ripple, Synchronous, Asynchronous, arbitrary, ring)
- Registers (Shift, Bidirectional shift, Parallel load)
- RAM (Static, Dynamic, RAM cells, address decoding, read/write, bit slice model)
- PLDs (ROM, PROM, PLA, PAL)
- VHDL
- Register transfers and Data Paths (registers, buses, ALU, micro-operations,)

STUDENT RESPONSIBILITIES:

- The Student must pass the theory/concepts portion of the course in order to obtain a passing grade for the term. In other words, a student must obtain 35 out of a possible 70 exam based marks - which includes all components except the lab assignments.
- LAB attendance is **mandatory**. You must clear all absences with me; failure to comply will result in a failing grade for the course!

STATEMENT ON PLAGIARISM AND CHEATING:

Cheating and plagiarism will not be tolerated and there will be penalties. For a more precise definition of plagiarism and its consequences, refer to the Student Conduct section of the College Admission Guide at http://www.gprc.ab.ca/programs/calendar/ or the College Policy on Student Misconduct: Plagiarism and Cheating at www.gprc.ab.ca/about/administration/policies/**

**Note: all Academic and Administrative policies are available on the same page.